Using the HI7188 to Create a 64 Channel Multiplexed System

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Introduction

The purpose of this application note is demonstrate the power and flexibility of the HI7188 to create a differential 64 channel A/D system. The HI7188 will perform all multiplexer switching control and calibration. This will enable the designer to perform a high precision 16-bit analog to digital conversion using one HI7188 sigma delta converter with up to sixty-four fully differential inputs. The 64 multiplexer channels are divided into 8 multiplexer blocks, with one block of 8 logical channels active at any given time. The conversion rate is 240 conversions per second per logical channel for each of the eight active channels. PGIA gain, unipolar/bipolar operation or calibration is on a per logical channel basis.

Functional Description

The HI7188 multiplexing circuit is shown in Figure 1. This includes the HI7188 Sigma-Delta A/D converter, (8) HI507 eight channel differential multiplexers and the (8) HA5102 dual ultra-low noise operational amplifiers.

A fully differential circuit was used to offer the greatest amount of noise immunity and common mode rejection. This type of circuit will only measure the difference between the HI and LO inputs. Noise voltage which is common to both signal lines will cancel out in this balanced differential amplifier. In addition, common mode voltages appearing at the inputs will also be rejected based on the amplifiers Common Mode Rejection Ratio (CMRR). Although differential inputs minimize the effects of noise, proper signal conditioning should be performed (i.e., twisted-pair, isolation, filtering).

Circuit Description

The inputs of this circuit begin at the HI507 which is a 8 channel differential multiplexer. The differential signal is applied and stable, for each channel, with the HI7188 performing all channel switching via the address pins A_2,A_1 and A_0. Due to the settling time of this circuit the HI7188 must be in line noise rejection (LNR) mode. In LNR mode the inputs have 54.6µs to switch/settle while in non LNR mode only 14.6µs. Please refer to the external multiplexing section of the HI7188 datasheet. The differential multiplexer outputs labeled OUTA and OUTB are then connected to the non inverting inputs to the dual HA5102 operational amplifiers. The op amps are used in unity gain to buffer the inputs of the HI7188 and to reduce the loading of the HI7188 differential inputs. In addition, the multiplexer on resistance (R_{ON}) varies with applied voltage. If left unbuffered this change of R_{ON} will cause linearity errors. The op amp has been designed for ultra low noise (4.3nV/$\sqrt{Hz}$) applications and a high CMRR (95dB). The op amp outputs are then connected to the HI7188 differential inputs labeled V_{INHI} and V_{INLO}. This basic cell of Multiplexer and Op Amp buffers are repeated for all eight HI7188 differential inputs as shown in Figure 1.

Power Supplies

This application circuit is designed to use ±5V for the HI7188 supply and ±15V for the multiplexers and op amps. With these increased op amp supplies, care should be taken to ensure the inputs of the HI7188 do not exceed the HI7188 supplies, or permanent damage may occur. The analog and digital supplies and grounds are separate on the HI7188 to minimize digital noise coupling into the analog circuitry. Nominal supply voltages are AV_{DD} = +5V, DV_{DD} = +5V, and AV_{SS} = -5V. If the same supply is used for AV_{DD} and DV_{DD} it is imperative that the supply is separately decoupled to the AV_{DD} and DV_{DD} pins on the HI7188. Separate analog and digital ground planes should be maintained on the system board and the grounds should be tied together back at the power supply.

System Flow and Control

The overall system flow is shown in Figure 2. The flow chart contains the basic steps to control the multiplexed system. It begins with the initial system start. Please refer to the “Using the HI7188” section of the datasheet. The control of this circuit is achieved by programming the Control Register (CR) and Channel Configuration Registers (CCR). The CR is 16 bits wide and contains information that determines operating mode and the system/chip level configuration. This configuration applies to all 8 logical channels and cannot be modified at the channel level. The CCR comprise a 64-bit (8 bits/channel) memory element that defines the logical channel conversion order as well as each logical channel specific data such as physical channel address, mode, gain, and bipolar/unipolar operation.

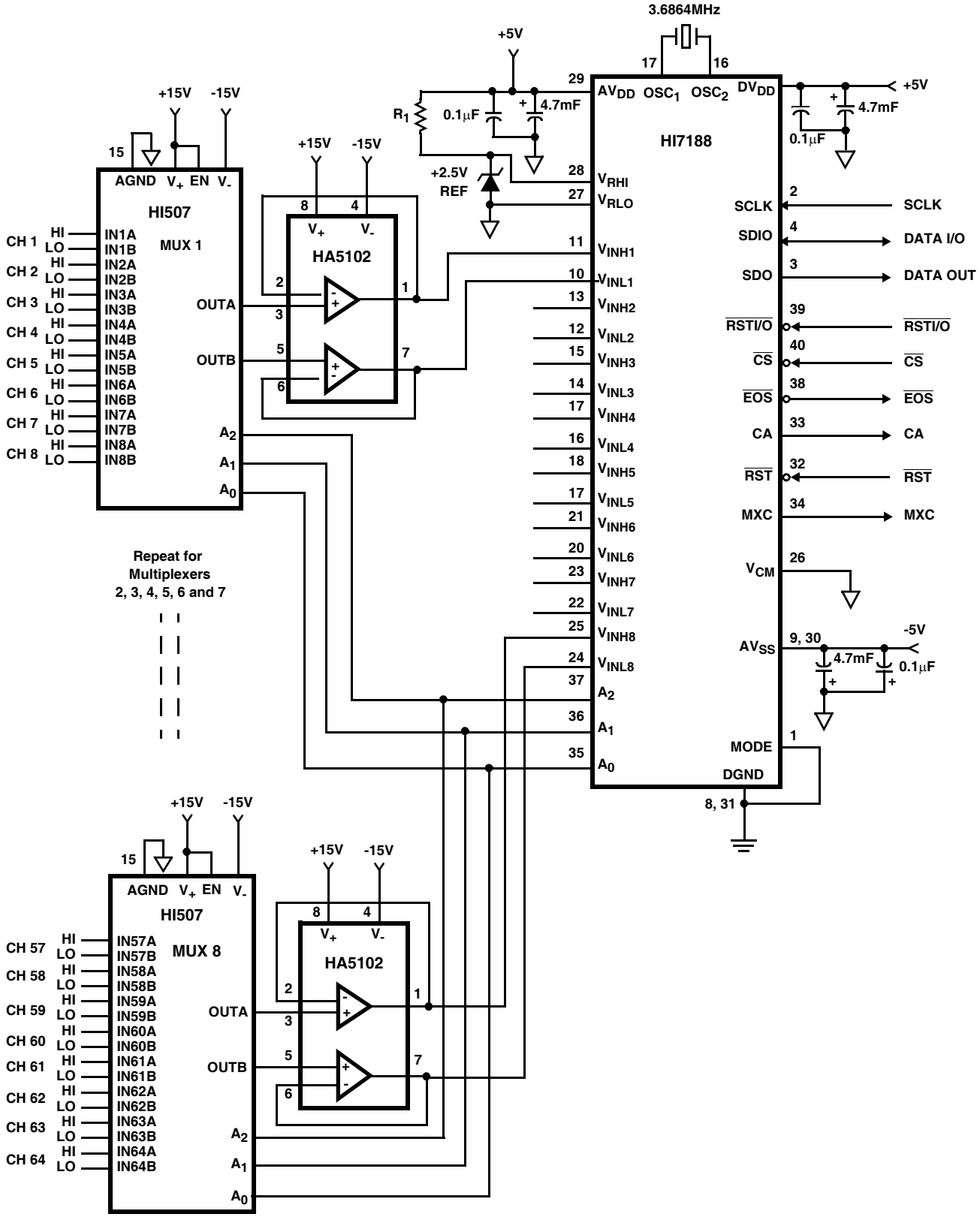

FIGURE 1. HI7188 MULTIPLEXING CIRCUIT

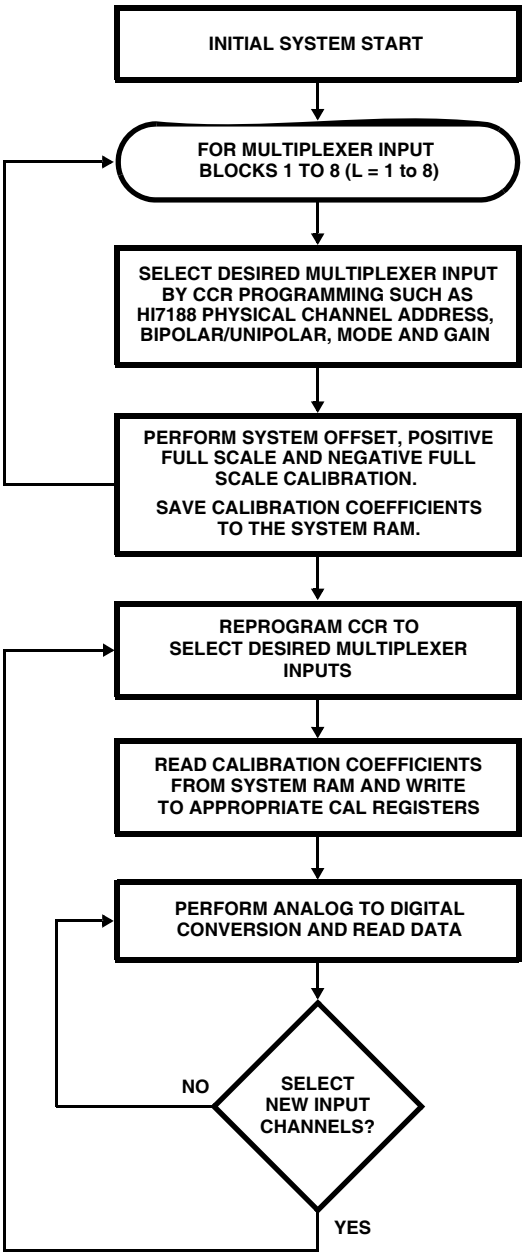

FIGURE 2. SYSTEM FLOW CHART

NOTE: Any change in ambient temperature, supply voltage or channel programming (outside of original channel calibration) the user should begin at the “initial system start” block

The CR functionality is well covered in the datasheet so it will not be discussed in this application note. The focus will be on the CCR programming since the multiplexer selection is defined by these registers for this application. It is therefore critical the user is well versed in the use of the CCR [1]. From the CCR the physical channel address, calibration, PGIA gain and unipolar/bipolar mode are set. For multiplexer selection, the particular logical channel bits of interest are 7, 6, and 5 which set the physical channel address. The physical channel address is used to select the proper multiplexer block shown in Figure 1. During the conversion scan, the microsequencer steps through each of the eight logical channels and provides the multiplexer address correlating to the proper logical address. When in LNR mode, the microsequencer provides this addressing function for eight channels regardless of the number of active channels defined in the CR. This is done to maintain LNR timing. Once again, this application will only work in LNR mode due to the settling time of the multiplexer and opamps.

Below are examples to demonstrate the use of the “physical” bits of the CCR byte to select different multiplexer blocks. These examples assume the calibration RAMs, as defined

later in the Calibration section, are updated and the CR is programmed correctly. In addition, the other bits of the CCR byte are don't care for these examples. Any unused muliplexer inputs should be connected to analog ground.

Example 1. The table below shows a simple use of the CCR to select MUX1 for all eight logical channels. The selection of MUX1 is achieved by setting the address bits <7:5> to logic zero. As defined in the Datasheet, this selects V_{INH1}, and V_{INL1} for all eight logical channels. The microsequencer changes the multiplexer channels automatically, in addition to, data coding and calibration.

Example 2. The Example 2 table shows a more complex use of the CCR to select several MUXs for the eight logical channels. This example also assumes the calibration RAMs, are updated for these inputs. The microsequencer changes the multiplexer channels automatically, in addition to, data coding and calibration.

It should also be noted that the channel order is not as flexible when using external multiplexers as when the internal HI7188 multiplexer is used. When the internal multiplexer is used, the physical channel order "skip and repeats" are totally programmable by the user. Since the logical address outputs are used to drive external multiplexers, the channel selected is directly tied to the logical channel decoder.

Calibration

The HI7188 has the ability to null any system offset errors and generate the positive and negative gain slope factors for the transfer function of the converter. The system offset and gain errors are nulled by performing a three point calibration which involves recording conversion results for three different input conditions - "zero-scale," "positive full-scale," and "negative full-scale".

Calibration should be performed for EACH of the logical channels for all eight multiplexers to null out the individual channel errors with the results stored in the microprocessor memory. Please refer to the HI7188 datasheet. When the user selects the desired multiplexer, via the CCR, the calibration coefficients should be read from the microprocessor memory and written back to the HI7188. A calibration routine should be initiated whenever there is a change in the ambient operating temperature or supply voltage.

EXAMPLE 1.

LOGICAL CHANNEL	BLOCK/ BITS	CH2 7 MSB	CH1 6	CH0 5	B/$\overline{U}$ 4	MD1 3	MD0 2	G1 1	G0 0 LSB	MULTIPLEXER BLOCK SELECTED	MULTIPLEXER INPUT SAMPLED
1	CCR2 <31:24>	0	0	0	X	X	X	X	X	MUX 1	CH 1
2	CCR2 <23:16>	0	0	0	X	X	X	X	X	MUX 1	CH 2
3	CCR2 <15:8>	0	0	0	X	X	X	X	X	MUX 1	CH 3
4	CCR2 <7:0>	0	0	0	X	X	X	X	X	MUX 1	CH 4
5	CCR1 <31:24>	0	0	0	X	X	X	X	X	MUX 1	CH 5
6	CCR1 <23:16>	0	0	0	X	X	X	X	X	MUX 1	CH 6
7	CCR1 <15:8>	0	0	0	X	X	X	X	X	MUX 1	CH 7
8	CCR1 <7:0>	0	0	0	X	X	X	X	X	MUX 1	CH 8

EXAMPLE 2.

LOGICAL CHANNEL	BLOCK/ BITS	CH2 7 MSB	CH1 6	CH0 5	B/$\overline{U}$ 4	MD1 3	MD0 2	G1 1	G0 0 LSB	MULTIPLEXER BLOCK SELECTED	MULTIPLEXER INPUT SAMPLED
1	CCR2 <31:24>	0	0	0	X	X	X	X	X	MUX 1	CH 1
2	CCR2 <23:16>	0	0	1	X	X	X	X	X	MUX 2	CH 10
3	CCR2 <15:8>	0	1	0	X	X	X	X	X	MUX 3	CH 19
4	CCR2 <7:0>	0	1	1	X	X	X	X	X	MUX 4	CH 28
5	CCR1 <31:24>	1	0	0	X	X	X	X	X	MUX 5	CH 37
6	CCR1 <23:16>	1	0	1	X	X	X	X	X	MUX 6	CH 46
7	CCR1 <15:8>	1	1	0	X	X	X	X	X	MUX 7	CH 55
8	CCR1 <7:0>	1	1	1	X	X	X	X	X	MUX 8	CH 64

Switching between Multiplexers

To obtain the new multiplexer/channel information the following bytes are transferred from the microprocessor memory. Please refer to the HI7188 datasheet for details of the Serial Interface.

NUMBER OF BYTES	REGISTER	COMMENTS
1	IR	Defines Pending 2 Byte CR Write
2	CR	Reprograms the HI7188
1	IR	Defines Pending Multi-byte Offset Calibration RAM Write
24	OC RAM	Offset Calibration Coefficients
1	IR	Defines Pending Multi-byte Positive Full Scale Calibration RAM Write
24	FS + RAM	Full Scale Calibration Coefficients
1	IR	Defines Pending Multi-byte Negative Full Scale Calibration RAM Write
24	FS + RAM	Full Scale Calibration Coefficients
78 (624 Bits)		Total

External Clocking Mode

If the HI7188 is in the external clocking mode [1] with the maximum serial interface clock of 5MHz. This sets the bit transfer to 1/SCLK = 200ns. The total “reprogramming” would then take 200ns x 624 bits = 124.8μs.

Self Clocking Mode

If the HI7188 is in the self clocking mode, the serial interface clock would be 460.8kHz. This sets the bit transfer to 1/SCLK = 2.17μs. The total “reprogramming” would then take 2.17μs x 624 bits = 1.35ms.

Measured Performance

The multiplexer and op amp portion of Figure 1 was built using a standard single-sided breadboard. The output of the op amps were then connected the HI7188 evaluation board [2] using 8 inch twisted pair wires. Testing of the overall circuit performance included both noise and linearity. The noise measurements consisted of grounding the HI507 inputs and datalogging 100 conversions. The peak to peak noise is defined as the difference between the minimum and maximum measured values. Linearity testing involved incrementing the input voltage in 0.5V steps starting with -2.495V and ending at +2.495V. The linearity error is the difference between the input voltage and displayed conversion results. There was no degradation in performance of either noise or linearity seen in this application circuit versus just the HI7188 evaluation platform.

Conclusion

In conclusion, this application note described the use of the HI7188 to create a 64 channel differential system. The functional and circuit description was detailed to describe the system. In addition, the system control and flow was discussed to explain the software control of the circuit.

References

[1] HI7188 Data Sheet, FN4016, Intersil Corporation

[2] Using The HI7188 Evaluation Kit, AN9518, Intersil Corporation